U. S. ARMY SIGNAL CENTER AND FORT GORDON
Fort Gordon, Georgia 30905-5180

LESSON PLAN

TITLE: AN/TYC-39A Communication Interface Group (CIG)

LEARNING OBJECTIVE:

Action: The student will describe the CIG functions and will perform CIG maintenance, which will include removal and replacement procedures.

Conditions: The student is given TM-11-5805-790-12 series, TM-11-5805-790-34 series and Practical exercise 150-74G10/E01-LP1.

Standard: The student has met the learning objective when he or she can correctly answer 14 out of 20 questions in 1 hour.

SAFETY CONSIDERATIONS: There are no safety consideration for this lesson plan.

RISK ASSESSMENT: A risk assessment has been conducted on this unit of instruction and the risk level is deemed to be: LOW RISK.

TIME: 18 Hours

RESOURCE NEEDS/ REFERENCES: AN/TYC-39A, Overhead Projector, Slides 1-32, Chalkboard, TM-11-5805-790-12 series, TM-11-5805-790-34 series, and practical exercise 150-74G10/E01-LP1.

METHOD OF INSTRUCTION: Conference

APPROVAL DATE: 2 DEC 97
DEVELOPER: SFC CARTAGENA
DIV. CHIEF: Jack P. Rondon

INSTRUCTOR NOTES:

1. Ensure that the classroom is available and properly set up and that all equipment and training resources are available and in working order.

2. Ensure that enough technical manuals are available and account for all transparencies.

3. Before the end of class, evaluate students on their ability to perform the learning objective.

4. State all safety notes as they appear throughout the lesson plan.

INTRODUCTION:

Elapsed Time

To successfully operate the AN/TYC-39A, you need a good working knowledge of the CIG. In this lesson, we will study the functions and interfaces of the CIG.

BODY:

5M

1. Communications Interface Group (CIG) Overview.

NOTE: Refer students to TM 11-5805-790-12-1 para 1-35, pages 1-64, 1-65, 1-13, and 1-14 Message Switching Central AN/TYC-39A Block Diagram, and discuss placement of the CIG within the message switch.

a. The CIG provides the interface between both dedicated and switched digital, unencrypted loops and trunks and the Message Processor (MP).

b. The loops/trunks can be data terminals, other message switches, or AUTODIN switches.

c. The CIG performs the following functions.

(1) Terminates TRI-TAC line types I, II, III, and IV subscribers.
(2) Converts bit serial subscriber line-side message data to message blocks.
(3) Performs code conversions for line type I.

(4) Monitors input data to determine when character and/or crypto synchronization have been lost.
(5) Monitors modem and crypto alarms and provides status information to the MP.
(6) Provides timing.
(7) All message characters, transferred between the CIG and the MP, use the odd-parity ASCII character format.

d. The CIG is made up of the following subgroups.

NOTE: Show Slide 1.

(1) Thirteen Intelligent Line Interfaces (ILIs) - Each ILI consists of three or four Line Termination Units (LTUs) and one Intelligent Line Interface Processor (ILIP). LTUs may be one of three types.

(a) Digital Line Termination Unit (DLTU).
(b) Data Adapter Termination Unit (DATU).
(c) Common Equipment Facility (CEF) Control Interface Unit (CCIU).

(2) Two redundant Digital Line Concentrators (DLCs) - Each DLC consists of two Line Cluster Functions (LCFs), a DLC Processor (DLCP), and an MP/DLC Link (MDL).
(3) Two redundant Master Timing Generators (MTGs).

(a) Provides all timing reference signals required by ILIs, TDIGM, CPG, and modems.
(b) Contains clock generation unit.
(c) Two modes of operation.

1. Slaved to a timing signal recovered by the group modem in TDIGM.

2. Independently driven by its own crystal oscillator.

1H

e. CIG data flow.

NOTE: Show Slide 2.

(1) LTU.

(a) Receives digital serial unencrypted data from LKG.
(b) Synchronizes to line and recovers data characters from bit stream.
(c) Organizes incoming bit serial data into character bytes.
(d) Raises Service Request Flag to ILIP.
(e) Transmits character bytes as bit parallel data to ILIP when instructed by ILIP.

(2) ILIP.

(a) ILI Bus provides multiplexing of up to four LTUs to a single ILIP.
(b) Scans LTUs for Service Requests.
(c) Reads data from each LTU.
(d) Collects and stores data into line blocks.
(e) Sends line blocks and control information, in network layer frames, to the LCF. The link layer of this interface employs a packet (X.25) protocol which provides for the exchange accountability and automatic repeat request of generic information frames (X.25 LAPB framing).

(3) LCF.

(a) The LCF is an input/output multiplexer that routes message data, control messages, and program segments between the ILIs and the DLCP.

(b) Receives the line blocks from a particular ILIP.
(c) Strips off X.25 framing.
(d) Transfers information to the DLCP in the order they are received from the ILIs via a multibus II protocol.

(e) The multibus II protocol provides a mechanism for the transfer of packets between the LCF and the DLCP. A packet is any block of information which is transmitted with a single transfer operation.

(4) DLCP.

(a) Collects status and data entities from the ILIs (via the LCFs).
(b) The entities collected may consist of line blocks, program download segments, status, control, or commands.
(c) Strips off multibus II framing.
(d) Transfers information to the MDL.

(5) MDL

(a) MDL is the link to the message processor.
(b) Translates data format because the DLCP and MP have different bus and data structures.
(c) Controls and coordinates the transfer of information between the DLCP and the MP. The information transferred is of three types.

1. Status Information.
2. Command Words.
3. Entities.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

QUESTIONS: How many ILIs are there in the message switch? (ANS: 13.)

How many LTUs interface with a single ILI? (ANS: 3 or 4, max is 4.)

2H 15M

2. Intelligent Line Interface (ILI) Overview.

NOTES: Show Slide 3.

Refer to TM 11-5805-790-12-1 para 1-36 page 1-67 para a & b.

a. The CIG is equipped with 13 ILIs to interface 48 lines, the MCS, and the two ICUs.

b. The ILIs are the CIG interface to the subscriber and trunk lines.

c. Each ILI converts the bit-serial line side terminal interfaces to a serial line block interface for the DLC.

d. There are three LTU types to interface with all subscriber types and to control and monitor the line conditioning equipment.

(1) Digital Line Termination Unit (DLTU) (DLTM6).

(a) Provides an interface for TRI-TAC Line Types I, II, and III lines and trunks.
(b) One DLTU provides the interface for the Modem Control and Status (MCS) function.

(2) Data Adapter Termination Unit (DATU) (DLTM9) - Provides an interface with TRI-TAC line Type IV lines and trunks.
(3) CEF Control Interface Unit (CCIU) (DLTM7 and DLTM8) - One CCIU provides the interface for each of two ICUs for

control and monitoring of the COMSEC equipment.

NOTE: Refer to TM 11-5805-790-12-1 para 1-35 page 1-65 and TM 11-5805-790-12-6 para 7-24 page 7-50.

e. Each ILI is comprised of an Intelligent Line Interface Processor (ILIP) and up to four LTUs.

(1) ILI1.

(a) Two DLTM6 or DLTM9 (any combination) (2 LTUs).
(b) One DLTM6 (for MCS).
(c) One DLTM7/8 (CCIU for ICU).

(2) ILI4.

(a) Two DLTM6 or DLTM9 (any combination) (2 LTUs).
(b) One spare slot.
(c) One DLTM7/8 (CCIU for ICU).

(3) ILIs 2, 3, and 5 through 13 - Contain four DLTM6 or DLTM9 circuit cards (any combination) (44 LTUs).

NOTES: Show Slide 4.

Refer to TM 11-5805-709-12-1 para 1-36 page 1-67.

f. The ILI performs the following functions for each loop and trunk interface.

(1) Line synchronization.
(2) Character recovery/transmission.
(3) Recognition of special control characters.
(4) Generation of message block parity.
(5) Forward error correction.
(6) Rate conversion.
(7) Framing.
(8) Conversion of incoming line codes to ASCII.

(9) Block assembly/disassembly.
(10) Automatic Repeat Request (ARQ) procedures.
(11) Detection and processing of character/COMSEC synchronization loss.
(12) Immediate storage for incoming and outgoing message traffics.
(13) Throttling.
(14) Loopback testing.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

QUESTIONS: What converts the bit serial line side terminal interfaces to a serial line block interface for the DLC? (ANS: ILI.)

Which ILI contains the CCIU for the ICU B? (ANS: ILI4.)

What DLTM cards make up the CCIU for the ICU? (ANS: DLTM 7 and 8.)

3H 5M

3. ILI Functional Description.

NOTE: Show Slide 5.

Refer to TM 11-5805-709-12-1 page 1-21 and page 1-89 para b & c.

a. Intelligent Line Interface Processor (ILIP).

(1) Each ILI contains an ILIP circuit card.
(2) The ILIP circuit card contains an 80386DX microprocessor supported by the required interface and memory devices.
(3) The ILIP acts as a buffer between the message oriented MP/DLC interface and the character oriented LTU interface.
(4) The ILIP provides an interface between the DLCs and the LTUs.
(5) Each ILIP is connected to both DLCs via Dual Channel Switch (DCS) circuitry.

(6) The ILIPs are configured to one DLC or the other in accordance with commands from the CAP.
(7) The ILIP connects to the LTUs via the ILI bus.
(8) The ILI bus provides multiplexing of up to four LTUs to a single ILIP.
(9) Each ILIP receives a 3.072 MHz clock from the Master Timing Generator (MTG) which is used to generate all the clocks required by the LTUs.
(10) The ILIP monitors, controls, and services the LTUs.
(11) The ILIP performs a sequential scan to collect the state and incoming data from each of the four connected LTUs.
(12) Output data is routed to the four LTUs after the scan cycle.
(13) The ILIP is responsible for the following functions.

NOTE: Show Slide 6.

Refer to TM 11-5805-709-12-1 page 1-67 and 1-87.

(a) Channel Control and Coordination - ILIP ensures that the transfer and receipt of message data is properly coordinated with the transfer of command and control characters to/from the LTU.
(b) Assembles incoming characters into message blocks - All message data is assembled into line block entities and formatted before transmission to the DLC.
(c) Forwarding of incoming line blocks to the DLC.
(d) Reception of outgoing line blocks from the DLC.
(e) Transmission of outgoing line blocks to LTUs as a character stream.
(f) DLTM 6 in slot 4 of ILIP nest: Monitor and Control Modems - ILIP

receives modem commands through the DLC, carries out the commands through the MCS via a DLTU, and reports response information back to the originator through the DLC.

(g) DLTM 7 & 8 in the ILIP nest: Monitor and Control LKGs - ILIP receives COMSEC commands through the DLC, carries out the commands through the ICU via a CCIU, and reports response information back to the originator through the DLC.

(h) Exchange of equipment status and control information with the MP.

(i) Generates all clocks required by the LTUs from the master timing source.

NOTES: Show Slide 7.

Refer to TM 11-5805-790-12-1 para 1-38 page 1-87.

(15) Major Functional Components. The ILIP consists of four functional sections that, together, provide the processing and interfaces required to control and route data to and from the associated LTUs. The functional sections are DLC Interface, ILI Bus Interface, Processor, and LTU Clock Generator.

(a) DLC Interface.

1. The ILIP/DLC interface transfers a full-duplex serial I/O data stream between the serial port of the processor and one of the two DLCs.
2. A Dual Channel Switch (DCS) under the direction of the Control and Alarm Panel (CAP) selects the DLC via the ILIP.
3. The two identical DLC interfaces provide full-duplex data paths for information exchange and an output clock

between the ILIP and the redundant DLCs.

4. A 64-Hz clock is supplied to the DLC interface by the serial communications controller.
5. Message data received from the line interfaces is processed by the ILIP. The received data is assembled and multiplexed into line blocks for transmission to the DLC.
6. When the DLC outputs data to the ILI, it distributes line blocks to the addressed ILIs, which demultiplex and disassemble the data to be transmitted by the individual line interfaces.
7. Data is exchanged between the ILI and the DLC using X.25 Link Access Procedures, Balanced (LAPB). This interface can be described in terms of layers: physical (layer 1), link (layer 2), and network (layer 3).

4H 20M

Refer to TM 11-5805-790-12-1 para 1-38 page 1-89.

(b) ILI Bus Interface.

1. The ILI bus interface provides for the transfer of data between the ILIP and the LTUs.
2. A scanner collects the state and incoming data from each of the four connected LTUs.
3. Input data is transferred byte parallel to the ILIP.
4. Output data is routed to the four LTUs between scan cycles.

5. The ILI interface with the LTUs is half-duplex, such that four LTUs are maintained in continuous full-duplex, 16-kb/s traffic. The clocks required by the LTUs are generated by the LTU clock generator in the ILIP.

6. Data Input:

   a. The ILIOP (ILI Operational Program) initiates and sets the input DMA channel for a 16-byte transfer from the scanner.
   b. Data is input from the four LTUs during each scan cycle.
   c. The scan cycle is initiated when the interface logic receives a pulse from the Programmable Interval Timer (PIT).

7. Data Output:

   a. Data is output when available and when the ILI interface logic is not performing a scan cycle.
   b. Output data is generated from two sources: DMA channels and programmed output.

      [1] DMA - There are four dedicated output DMA channels (one for each line). Blocks of data are

transferred via these channels.

[2] Programmed Output - for downloading classmarks, transferring commands and control characters to the LTUs, and terminating transmissions.

(c) ILIP Processor.

The ILIP processor includes a 32-bit Intel 80386-microprocessor device with a minimum operating cycle of 16 MHz. It processes program instructions from the ILI Operational Program (ILIOP) to meet the interface conversion and intermediate storage requirements of the ILIP. The processor includes memory, programmed I/O, direct memory access control, serial communication control, interrupt control, Built-in Test (BIT), and programmable interval timing functions. The processor is supported by a 32-bit bus structure.

1. Memory - Memory consists of both Random Access Memory (RAM) and Read-Only Memory (ROM).

a. The RAM is used for ILIOP program code storage and protocol data buffering. The capacity is 128K 32-bit words.

b. The ROM is used to store the ILIOP program load and diagnostic functions.

The capacity is 64K 16-bit words.

2. ILIP Operational Program (ILIOP)

a. The ILIOP provides control and processing for the ILIP.
b. It helps to provide distributed communications processing for the message switch by facilitating the transfer of data between the DLC and the external subscriber lines, COMSEC, and modems.
c. The ILIOP also performs security checks, converts between character formats, and throttles data on both the line and DLC interfaces when necessary.
d. The ILIOP exchanges commands and status with the DLC and the line side hardware. These allow the ILIOP to monitor and control the line side hardware, allow the DLC and MP to monitor and control the ILIOP, and allow ILIs to communicate with each other.

5H 10M

3. Direct Memory Access (DMA) Channels.

a. Five DMA channels support the ILI bus interface. Four are used for transmit data; one is used for receive data.
b. Two DMA channels support the DLC interface. One is used for transmit data;

the other is used for receive data.

NOTE: Refer students to TM 11-5805-790-12-1 page 1-91.

4. Serial Communication Controller (SCC).

   a. The SCC provides full-duplex serial data exchange between the DLC interface and the ILIP processor.
   b. Two DMA channels support the I/O data channels between the SCC and the processor.
   c. The DMA channels and the SCC interrupt the ILIP processor to signal I/O completion and/or error conditions.

5. Programmable Interval Timer (PIT).

   a. The PIT provides the ILIOP with programmable interval timers.
   b. The interval timer provides its current count to the ILIP processor upon request.
   c. It also provides an interrupt to the ILIP processor via the interrupt controller at the end of the programmed interval.
   d. The interval timer period is programmable up to 65 ms in increments of 1 ms.
   e. The direct output of one timer is supplied to the ILI bus interface for the

initiation of each scan cycle.

6. Interrupt Controller - The interrupt controller collects and prioritizes interrupts from the following functions in the order listed.

   a. PIT1.
   b. PIT2.
   c. CAP select lines.
   d. Direct memory access channels.
   e. Serial communications controller.
   f. ILI interface logic.

7. CPU Timing.

   a. CPU timing is provided by the processor clock.
   b. The processor clock is an independent, crystal-controlled clock generator which runs at the frequency required to operate the ILIP processor.
   c. This clock generator is used for all of the ILIP except the LTU clock generator.

(d) LTU Clock Generator.

1. The LTU clock generator generates the clocks required for LTU operation.
2. The LTU clock generator receives a 3.072-MHz clock from the Master Timing Generator (MTG).

3. The LTU clock generator generates 76.8 kHz, 32.0 kHz, 4.755 kHz, 3.640 kHz, 3.200 kHz, 2.909 kHz, and 56.89 kHz.

(16) The MCS and modem control function is accomplished by the ILIPs.

NOTE: Show Slide 8.

(a) They can be controlled manually via the switch supervisor in response to an equipment command.

NOTE: Show Slide 9.

(b) Or, they can be controlled automatically via the ILI servicing the modem in response to a route command.

(17) COMSEC equipment (ICUs, LKGs, TEDs, and RCUs) is controlled by the ILIPs.

NOTE: Show Slide 10.

(a) COMSEC equipment can be controlled manually via the switch supervisor in response to an equipment command.

NOTE: Show Slide 11.

(b) It can also be controlled automatically via the ILIP servicing the COMSEC equipment in response to a route command.

NOTE: Refer students to TM 11-5805-790-12-1 para 1 37a, pages 1-70.

b. LTUs.

(1) DLTU (DLTM6).

NOTE: Show Slide 12.

(a) The DLTU provides the MS interface to TRI-TAC line types I, II, and III loops and trunks.

(b) The DLTU line side interfaces with the LKG, which terminates the loop or trunk interface.

(c) The DLTU transmits and receives unencrypted data to and from the LKG. This data is serial binary.

(c) Subscribers may be ASCII of either parity or ITA No. 2 format. Therefore, conversion to ASCII may be necessary.

(e) The switch side of the DLTU interfaces with the ILIP.

6H 25M

(f) The DLTU also accepts commands from the ILIP. This allows the ILIP to control the DLTU operation.

(g) The DLTU also accepts ILIP classmarks. These classmarks define the characteristics of lines connected to the DLTU. Classmarks consist of two 16-bit words sent to the DLTU from the ILIP.

(h) The DLTU has two basic sections: a transmitter and a receiver. They are controlled by the DLTU controller. They control data flow between the ILIP and the line.

1. The DLTU transmitter receives messages and control characters from the ILIP. It transmits them to the line in a bit serial fashion. The transmit selector determines the source of a character. It does this under the control of the DLTU controller. It loads the character into the transmit register.
2. The DLTU receiver accepts bit serial data stream from the COMSEC unit, which ends the loop or trunk interface.

NOTE: Refer students to TM 11-5805-790-12-1 para a, page 1-76.

(2) CCIU (DLTM7 and DLTM8).

NOTE: Show Slide 13.

(a) The CCIU provides the interface between the ILIP and the ICU.
(b) This interface permits the ILIOP to command the LKGs and TEDs to provide appropriate encrypt functions.
(c) The CCIU provides the ILIOP with the character-by-character processing required to issue commands and to receive status from the ICU.
(d) The CCIU receives ICU messages over the output serial data line at 32 kb/s.
(e) The CCIU converts the serial input bit stream into 9-bit characters. There are eight bits per parity.
(f) The CCIU loads the characters into the receive buffer after a parity check on each character. If wrong parity is found, the CCIU sends a status report to the ILIP.
(g) The receive buffer provides storage for a minimum of three 8-bit message characters. After a parity check at this time, the character parity bit is dropped, not sent to ILIP.
(h) When the first message character is input, processed, and stored in the receive buffer, message transfer to the ILIP begins.
(i) After the CCIU gets an ICU message, the CCIU inhibits any further input from the ICU until the full message is in the ILIP.
(j) The CCIU transfers the message one character at a time to the ILIP.

NOTE: Refer students to TM 11-5805-790-12-1 para c, page 1-78.

(3) DATU (DLTM9).

NOTE: Show Slide 14.

(a) The DATU is a software-programmable, plug-in module which provides a data interface between the character-oriented ILIP and a bit serial line.
(b) The DATU supports the message switch-to-circuit switch interface, other message switch trunks, and subscriber interfaces employing data adapters.
(d) Data access to the message switch for a TRI-TAC type IV line is accommodated on a full-duplex digital basis with a data adapter.

(d) The DATU establishes the transmission rate, information rate, forward error correction characteristics, framing, transmission mode, and character code parameters on line type IV loops and trunks.
(e) Each DATU provides service for one loop or trunk.
(f) The DATU receiver performs error correction and rate conversions required to recover characters from the bit serial line interface.
(g) The recovered characters are buffered and then transferred to the ILIP.
(h) The DATU transmitter receives characters from the ILIP and stores them for further processing. It performs encoding and rate conversion to make the characters compatible with the receiving device and transmits them bit serially on the line.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

QUESTIONS: What provides the ILIOP with programmable interval timers. (ANS: PIT.)

What card is the DLTU? (ANS: DLTM6.)

What card is the DATU? (ANS: DLTM9.)

7H 45M

NOTE: Refer students to TM 11-5805-790-12-1, page 1-67.

4. ILI Interface Description. The LTU organizes the incoming bit serial data into character bytes and transmits it as bit parallel data to the ILIP via the ILI bus. The ILIP collects and stores the characters into buffers as line blocks of 84 characters. These line blocks and control information are sent in network layer frames to the DLC selected by the CAP.

Outgoing data is routed through the same interfaces in the reverse direction. The external and internal interfaces are as follows.

NOTE: Refer students to TM 11-5805-790-12-1 para a, page 1-87.

a. ILIP/CAPC.

(1) The CAP interface report the status of the DLC to the Control and Alarm Panel (CAP) also allows the selection of one of the DLC. The selection is accomplished by a two-position, dual-channel switch in the ILI. The interface consists of two select, two status, and one reset line.
(2) Five signals form the CAP interface.

NOTE: Show Slide 15.

(3) Physical Interface.

NOTE: Refer students to Nest Map, and TM 11-5805-790-12-6 para 7-24, page 7-51 and discuss.

(a) The physical wiring to/from the ILIP is IAW the DLC/ILI NEST WRL.
(b) The ILI circuit cards are located in rows 5 and 6 of the DLC/ILI nest for the purpose of signal stringing.

1. Row 5.

a. ILIPs 1 through 7.
b. LTUs 0 through 23.
c. DLTU for MCS (504).
d. Both CCIUs (507 and 526).
e. 12V Regulator (519).

2. Row 6.

a. ILIPs 8 through 13.
b. LTUs 24 through 47.
c. 12V Regulator (619).
d. CAPC (640).
e. SCGRT (Resistor Terminator) (641).

NOTE: Refer students to TM 11-5805-790-12-1, page 1-67.

b. ILI-to-LKG.

(1) The ILI to LKG interface is subdivided into the DLTU-to-LKG and the DATU-to-LKG.
(2) The DLTU provides an interface for line and trunk types I, II, and III.
(3) The DATU provides an interface for type IV lines and trunks.
(4) Both the DLTU and DATU interfaces are used to transfer unencrypted (red) data and clock signals between an ILI and an LKG.

(5) The data can be synchronous or asynchronous and is programmable for a number of different baud rates.
(6) The two interfaces are identical except for allowable clock bit rates.

NOTE: Refer students to TM 11-5805-790-12-1, page 1-68.

c. ILI-to-MCS.

(1) The control and monitoring of modems is accomplished by the Modem Control and Status (MCS) function via a single DLTU.
(2) This interface consists of two signals: a command signal from DLTU to MCS and a status signal from MCS to DLTU.
(3) These signals carry serial, asynchronous bit streams using eight data bits, one start bit, and one stop bit.
(4) The data transmission rate is 4800 baud.

NOTE: Tell students that a more detailed discussion of the MCS interface will be covered in the MCS lesson.

9H 40M d. ILI-to-ICU.

(1) The control and monitoring interface for the COMSEC equipment is provided by two Interface Control Units (ICUs).
(2) Each ICU interfaces with a special LTU, called the CEF Control Interface Unit (CCIU).

(3) The CCIU interfaces to an ILIP.
(4) Each CCIU supplies a 32-kHz clock to the ICU to which data transfers are synchronized.
(5) Ready and acknowledge signals are used to transfer transmit data from the CCIU to the ICU and to receive data at the CCIU from the ICU.

e. ILI-to-LCF.

NOTE: Show Slide 16.

(1) Each ILI is connected to both redundant DLCs via ILIP to LCF interfaces.
(2) Each ILIP only communicates with one LCF, as determined by the CAP.
(3) Data is exchanged over this interface via a serial, full-duplex, synchronous communication channel. This interface can be described in terms of layers: physical, network, and link.

NOTE: Refer students to TM 11-5805-790-12-1, page 1-87.

(a) Physical Layer.

1. Provides for the electrical transfer of a synchronous bit stream across the interface.
2. The interface operates synchronously at 64 kb/s.
3. The physical interface is a full-duplex, synchronous information exchange.
4. Each ILIP connects with the DLC via send data signals, receive data signals, and transmit timing.

(b) Network Layer.

1. Identifies the type of entity being transferred.
2. Identifies the sender.
3. Verifies the receiver. (security validation)
4. Supports the disposition of the entity.

5. The network layer frame is transported within the link layer information field.

(c) Link Layer.

1. Provides the exchange, accountability, and Automatic

Retransmission Request (ARQ) for information frames as specified by the X.25 link access procedures.

2. The link layer information field transports the network layer as an envelope to the network layer.

3. The link layer protocol is symmetrical and, as such, the terms transmitter, receiver, and distant end may refer to either the DLC or the ILI.

(4) Physical Interface.

f. ILIP-to-LTU.

LTU-to-ILIP Clock (Signals) Description.

NOTE: Show Slide 17.

(1) CLKBN - CLOCK B 76.8 kHz CLOCK. This clock is used when terminating line interfaces operating at the following rates:

a. 9600 baud.
b. 4800 baud.
c. 2400 baud.
d. 1200 baud.
e. 600 baud.
f. 300 baud.
g. 150 baud.
h. 75 baud.

1. This clock is used with all line type I and II interfaces operating at the above rates.

2. This clock is used with line type III interfaces operating at the above rates if no transmit

clock is supplied by the COMSEC device.

3. This clock is used by the DATU to develop internal timing.

(2) CLKCN - CLOCK C 32.0 kHz CLOCK. This clock is used when terminating line type III interfaces operating at 16,000 baud if no transmit clock is applied by the COMSEC device. This clock is used by the DATU to develop internal timing. This clock is used by the CCIU to develop internal timing and to derive the 32 kHz clock supplied to the ICU.

(3) CLKDN - CLOCK D 4.755 kHz CLOCK. This clock is used when terminating line type I interfaces operating at 74.2 baud.

(4) CLKEN - CLOCK E 3.64 kHz CLOCK. This clock is used when terminating line type I interfaces operating at 56.9 baud.

(5) CLKFN - CLOCK F 3.2 kHz CLOCK. This clock is used when terminating line type I interfaces operating at 50.0 baud.

(6) CLKGN - CLOCK G 2.909 kHz CLOCK. This clock is used when terminating line type I interfaces operating at 45.45 baud.

(7) PAA - PHASE A of 56.89 kHz CLOCK. This clock provides one of the two clocks required by the DLTU MOS Logic circuits which process characters and information rate bits.

(8) PBA - PHASE B of 56.89 kHz CLOCK. This clock provides the second clock required by the DLTU MOS logic circuits which process characters and information rate bits.

g. ILIP-to-MTG - The Master Timing Generator (MTG) supplies each ILIP with a 3.072-MHz clock. A separate clock is provided for each of five groups of ILIs.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

QUESTIONS: What provides an interface for line and trunk types I, II, III? (ANS: DLTU.)

What row in the ILI nest contains ILIP 8 through 13? (ANS: Row 6.)

What card is located in row 6 slot 40 of ILI card nest? (ANS: CAPC card.)

10H 55M

NOTE: Refer students to TM 11-5805-790-12-1, page 1-92.

5. DLC Functional Description - The DLC consists of four circuit card assemblies: two LCFs, a DLCP, and an MDL.

NOTES: Refer students to TM 11-5805-790-12-1, page 1-94.

Show Slides 18,19 and 20.

a. LCF.

(1) The LCF is an input/output multiplexer that routes message data, control messages, and program segments between the DLCP and the ILIs.
(2) Provides a means for the DLCP to control, monitor, and exchange data with up to seven ILIs.
(3) Contains an 80186 Microprocessor supported by the required interface and memory devices.
(4) Operates under control of the LCF Operational Program (LCFOP).
(5) Acts as a buffer between the ILIP and DLCP.

(6) Provides a high-speed parallel data path between the DLCP and ILIs.

(7) Major Functional Components.

NOTE: Show Slide 21.

(a) Central Processing Unit (CPU).

1. An Intel 80186 microprocessor operating at 16 MHz.
2. LCF Operational Program (LCFOP).

a. LCFOP is the computer program operating within the CPU.
b. Provides control and processing for the LCF portion of the DLC.
c. LCFOP provides management of pooled memory to be used for the central storage of entities.
d. LCFOP provides a set number of buffers for the storage of output entities to each ILI.

(b) Memory.

1. Read-Only Memory (ROM).

a. 64K by 16 bits.
b. Used to support the boot programs required prior to the load of the operational software into Random Access Memory (RAM) and to support Built-In Self Test (BIST).

2. RAM.

a. 256K bytes of either static or dynamic RAM

b. Used to store data and the operational software, and for all other functions requiring memory.

c. Memory access is with zero wait states at a 16 MHz CPU operating cycle.

(c) Programmable Interval Timers (PITs).

1. Minimum of four independent PITs.
2. PITs used to generate timekeeping interrupts for real-time event processing by LCFOP.
3. The interval periods are adjustable over a minimum range of 5 ms to 100 ms in a granularity of at least 5 ms.

(d) Wait State Generator - Generates any delays which are necessary for the CPU to access any on-board devices.

1. Wait states are added so that the CPU can be slowed down while talking with other devices.
2. The adding of wait states is completely transparent to the LCFOP.

(e) Interrupt Controller.

1. Various devices which support the CPU in transferring data across the LCF's interfaces are capable of initiating an interrupt to LCFOP. These devices include:

a. Direct I/O processors (2).
b. Parallel System Bus (PSB) Controller.
c. PITs.

2. LCFOP contains a prioritized interrupt system.

(f) Direct Memory Access (DMA).

1. LCFOP contains, in hardware, a prioritized direct memory access transfer capability.
2. DMA transfers are handled by a DMA Controller.
3. LCFOP performs all necessary programming of this controller.
4. All DMA actions are initiated by the LCFOP.
5. Once DMA access is initiated, data is transferred between memory and a bus device without further LCFOP action.

(g) ILI Interface.

1. There are seven full-duplex synchronous serial interfaces with ILIs.
2. The link layer of this interface employs a packet (X.25) protocol which provides for the exchange account-ability and automatic repeat request of generic information frames (X.25 LAPB framing).
3. Serial Communication Controllers (SCCs).

a. Each LCF card have four SCCs. Each SCC support two ILIP cards. One LCF card contains eight SCC channels.
b. Minimize the processing required by LCFOP.

c. Capable of supporting the physical layer and some of the link layer of each interface.

(h) DLCP Interface.

1. LCF transfers input entities to the DLCP in the order they are received from the ILIs via a multibus II protocol.
2. Contains a PSB Controller (Message Passing Co-processor (MPC)).

a. Minimizes the processing required by LCFOP.
b. Controls the passing of all data over the multibus.

(i) Serial Interface.

1. RS-232C asynchronous serial interface.
2. Used for test purposes.
3. The speed of the interface is controllable through software strapping, consisting of one start bit and one stop bit, and allows for speeds of 300, 1200, 2400, 4800, or 9600 baud.

11H 50M

4. Used by depot facility for component level fault isolation.

NOTE: Refer students to TM 11-5805-790-12-1, page 1-96.

b. DLCP.

NOTE: Show Slide 22.

(1) The DLCP is a 32-bit microprocessor-based single-board computer.
(2) The DLCP is connected to an MP/DLC Link (MDL) and the Line Cluster Functions (LCFs).

(3) The DLCP, with its DLC Operational Program (DLCOP), is responsible for the transfer of commands, status, and data between the ILIs and the MP.
(4) The DLCP collects status and data entities from the ILIs and concentrates these into the MP (via the MDL).
(5) Major Functional Components.

(a) Central Processing Unit (CPU).

1. An Intel 386 microprocessor operating at 20 MHz.
2. DLCP Operational Program (DLCOP).

a. DLCOP is the computer program operating within the CPU.
b. The DLCOP collects status and data entities from the ILIs (via the LCF cards) and concentrates these into the MP (via the MDL).
c. The entities may consist of line blocks, program download segments, status, control, or commands

(b) Memory (both ROM and RAM) allows single-operation, 32-bit word transfers.

1. The ROM is 512K bytes and provides hardware and interface logic initialization, diagnostics, built-in self test, and program download.
2. The DLCP can reset its hardware and transfer control to ROM when directed by the MDL via the CSM.

3. The RAM is 2M bytes and provides operational program storage, data storage, buffering, and all other functions requiring temporary storage.
4. The memory is arranged to allow 32-bit single operation access by the CPU and the peripheral controllers.

(c) Clock Generator Unit.

1. The clock generator generates all the necessary timing signals for DLCP local operation.
2. It is an independent and self-contained unit.
3. It provides the CPU with a 20-MHz operating cycle.

(d) Direct Memory Access (DMA) Controller.

1. The DMA controller performs data transfers between main memory and I/O devices without CPU intervention.
2. The DMA channels are independent and can be prioritized.
3. Two DMA channels are used for the PSB interface.
4. One DMA channel is used for the SBX interface.

(e) Interrupts.

1. Various devices which support the CPU in transferring data across the DLCP's interfaces are capable of initiating an interrupt to DLCOP. These interrupts include:

a. Timers (PITs)

b. DMA (input/output)
c. Resets (power up/CSM)
d. SBX interface
e. PSB interface

2. The interrupt controller is programmed by DLCOP for both the priority of and masking of these interrupts.

(f) Programmable Interval Timers (PITs)

1. Minimum of four independent PITs
2. PITs are used to generate timekeeping interrupts for real-time event processing by DLCOP.
3. The interval periods are adjustable over a minimum range of 5 ms to 100 ms in a granularity of at least 5 ms.

(g) LCF Interface

1. The DLCP communicates with the LCF over a multibus II PSB bus in accordance with IEEE Standard 1296. This is a 32-bit wide data bus.
2. Central Services Module (CSM)

a. The CSM provides the bus management required by the Multibus II hardware implementation used in the design of the DLC.
b. The CSM performs all central control functions for the PSB multibus in accordance with IEEE Standard 1296.

12H 25M

(h) MDL Interface.

The DLCP communicates with the MDL via an iSBX bus in accordance with the functional and electrical specifications of IEEE Standard P959.

NOTE: Refer students to TM 11-5805-790-12-1, para 1-42 page 1-99.

c. MDL.

NOTE: Show Slide 23.

(1) The MDL controls and coordinates the transfer of information between the DLCP and the MP. These two devices have different buses and handle different data structures.
(2) The MDL provides the bit translation and data buffering required to accommodate the bit orientation and bus-length differences between the IOE and SBX buses.
(3) The entities transferred between the MP and the DLCP also require byte translation in certain cases.
(4) The information transferred is of three types.

(a) Status information - Supplied to both the DLCP and MP.
(b) Entities - Include all the types of information exchanged between the MP and CIG, other than the status and command words.

(5) The MDL functions as an input/output controller.
(6) It also acts as a data translator between the MP and the CIG processors.

(a) This is necessary due to the different way in which the two types of processors store data internally.

(b) To accommodate the two types, the MDL implements one of two translation algorithms: Last-In/First-Out (LIFO) and First-In/First-Out (FIFO).

(7) Major Functional Components

The MDL contains a Dual Channel Switch (DCS) consisting of the control/status circuit, IOE select logic, and two sets of driver/receivers.

1. This allows the CAP to select the IOE bus to either one of the MPs.
2. Status lines to the CAP keep the CAP informed of the current state of the switch.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

13H 10M

6. DLC Interface Description.

NOTE: Show Slide 24.

a. LCF/ILI.

(1) Send Data.
(2) Receive Data.
(3) Transmit Timing.

b. LCF/DLCP.

The multibus II protocol provides a mechanism for the transfer of packets (messages) between the DLCP and the LCFs. A packet is any block of information which is transmitted within a single transfer operation.

c. MDL/DLCP.

NOTE: Show Slide 25.

(1) The MDL controls and coordinates the transfer of information between the DLCP and the MP.
(2) Every entity transfer is initiated by the transfer of a command word (OFR word) from the MP to the DLCP.

d. MDL/MP.

(1) DEV Operation.

(a) The MP issues DEV commands to the MDL to set up and coordinate transfers between the MP and the MDL.
(b) Upon initialization, the MDL awaits the transfer of a command word from the MP.

e. MDL/CAPC.

(1) Five signals form the CAP interface.

(a) Two Select (active low) - Cause MDL to connect to one of two MP IOE bus systems.
(b) Two Status (active low) - Returned to CAP to indicate which IOE bus is selected.
(c) One Reset (active low) - Causes MDL to 'warm start', which causes MDL to initialize and an interrupt to be sent to the DLCP.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

13H 55M

7. MCS Overview.

NOTE: Show Slides 26 and 27.

a. The Modem Control and Status (MCS) is part of the Communications Equipment Support Group (CESG) of the Message Switch. It is co-located and interconnected with the modems.

b. The MCS is a remote multiplexer that provides the means for status monitoring and control of the modems.

c. The MCS provides a means of exchanging status and control information between the modems and the ILIs.

d. The MCS responds to commands received from the Intelligent Line Interface (ILI).

e. The ILIOP receives modem commands through the DLC, forwards the commands to the MCS via the DLTU, and reports response information to the originator through the DLC.

f. The MCS is capable of monitoring and/or controlling up to 48 modems.

g. The MCS sends commands to and receives status from each of the 48 modems.

h. The MCS provides the CIG with loopback control of the modems.

i. The MCS provides status reports on the modems and on itself to the ILI, either automatically or on command by the ILI.

j. The MCS is capable of receiving commands from the ILIP, via the DLTU interface, to perform modem loopback test, as well as MCS test.

Refer students to TM 11-5805-790-12-1, page 1-62.

NOTE: Show Slide 28.

k. The MCS has three basic functions.

(1) To scan the status lines of the modems and report the current condition of the lines when a change has been detected.

(2) To receive control information from the CIG and update the control line of the appropriate modem.
(3) To report the current condition of the status lines of a modem when requested by the CIG.

QUESTIONS: The MCS is part of what major group? (ANS: CESG.)

The MCS is capable of controlling and monitoring how many modems? (ANS: 48.)

14H 40M

8. MCS Functional Description.

a. The MCS is composed of three MCS Units (MCSUs).

NOTE: Show Slide 29.

b. These MCSUs are all of the same type and each occupy an individual CCA.

c. Backplane wiring allows each MCSU to determine its position within the MCS.

d. Each MCSU provides one third of the MCS's loop modem interface by interfacing with 16 of the modems.

(1) MCSU 0 - modems 0 through 15.
(2) MCSU 1 - modems 16 through 31.
(3) MCSU 2 - modems 32 through 47.

e. The reception channel of the MCS's ILI interface is common to all the MCSUs.

f. Only one MCSU may have control of the transmission channel at a time.

g. A master MCSU arbitrates bus control through the use of ILI interface control lines.

h. Each MCSU is composed of eight functional blocks. They are: ILI Interface Function, Loop Modem Interface Function, Command Decoder, Parity Checker, Parity Generator, Alarm Scanner, Status Formatter, and Self-Test Function.

Note: The following are sub-functions of the MCSU component.

(1) ILI Interface Transmission Arbitration.

a. Only one MCSU is allowed to transmit data to the ILI at a time.
b. The MCSU with the highest priority (the MCS can operate with one or more of its MCSUs missing) acts as master.
c. The master MCSU controls the other MCSUs access to the transmission path.
d. MCSU0 is assigned the highest priority and MCSU2 the lowest.
e. Eleven individual TTL ILI interface control lines are provided between all the MCSUs.
f. These lines allow an individual MCSU to determine whether it is the master or a slave and, depending on its role, to arbitrate or request access to the interface.
g. The interface control lines also allow recovery if an MCSU fails or is added to the MCS.
h. This information sheet describes the ILI interface control lines for each of the five possible roles an MCSU can fill.
i. Each MCSU must determine which of these roles applies to it by determining its location in the MCS (whether it is MCSU0, MCSU1, or MCSU2) and by monitoring the Card Present A and B lines.
j. If both lines are inactive, then the MCSU is the master; otherwise, it is a slave.

k. The ILI interface function of the MCSU informs the command decoder of whether it is master or slave.

l. When a slave MCSU wants to transmit on the ILI interface, it asserts its Bus Request line.

m. The master MCSU responds by asserting its Enable line to the requesting MCSU, providing the interface is not being used or is not already requested by another MCSU.

n. When the slave receives this Enable, it performs its transmission to the ILI.

o. When the transmission has been completed, it asserts its End Operation signal, which causes the master to de-assert the Enable line.

p. The master is responsible for fairly arbitrating access to the ILI interface between itself and the other MCSUs.

q. The master is responsible for maintaining the line in a Mark state whenever access is not granted to one of the other MCSUs (unless, of course, it is transmitting data itself.)

r. The slave is responsible for maintaining the line in a Mark state whenever access is granted to it (unless it is transmitting data.)

s. The master resets the bus by pulsing the Reset Request and Enable Lines A signal.

t. The receipt of this reset pulse causes all MCSUs to reset their Bus Request and Enable signals (if any are set) and to cease any transmission to the ILI.

u. This reset is performed under two conditions.

[1] When an MCSU becomes the master (e.g., if the original master fails or at power-up).
[2] When a slave MCSU does not return the End Operation signal within 10 ms of being granted the bus.

16H

(2) Command-Specific Processing.

a. Modem Loopback.

[1] Initiated by ECMD LPBM MODEM XX.
[2] This command causes the command decoder to notify the loop modem interface function to place the addressed modem into loopback mode.
[3] In the loopback mode, any baseband data sent to the modem for transmission is looped back on itself at the modem's analog interface.

b. Modem Normal.

[1] Initiated by ECMD RESET MODEM XX or by placing a channel in-service.
[2] This command does nothing if the modem is not in loopback mode already.

c. Modem Status Request.

[1] Initiated by ECMD REQS MODEM XX.
[2] This command causes the command decoder to notify the status formatter to format and send the address and status of the modem addressed.

d. MCS Test.

[1] Initiated by LPBK CHN 52 MCS or DIAG.
[2] Causes the command decoder to notify the self-test function to perform a self-test and then, when the results are received, to notify the status formatter to format and send the MCSU test results status word to the ILI.

e. MCS Reset - Initiated by CISR 52 or when DLC is initialized and causes the command decoder to:

[1] Put all modems in the normal mode.
[2] Notify the status formatter and alarm scanner of a reset condition.
[3] Notify the self-test function to perform a self-test.
[4] When the self-test results are received, notify the status formatter to format and send the MCSU test results status word to the ILI.

(3) Self-test Function.

(a) The self-test function initiates a self-check on power-up or after receiving an indication from the command decoder.
(b) This self-test checks the internal logic of the MCSU.
(c) The MCSU contains an LED, which lights momentarily and then goes off if the self-test passes.
(d) If this LED remains lit, it is an indication that the self-test failed.
(e) Once the self-test is completed, the self-test function reports the results to the command decoder.

QUESTION: What is the purpose of the self-test function? (ANS: The self-test checks the internal logic of the MCSU.)

16H 45M

9. MCS Interface Description - The MCS has two external interfaces, one with the ILI and one with each of the loop modems.

   a. ILI Interface.

   NOTE: Show Slide 30.

   (1) The ILI to MCS interface is a full-duplex, asynchronous, serial data transmission and reception channel.
   (2) This interface operates at 4800 baud and meets the electrical requirements of the balanced serial interface.

   b. Loop Modem Interface.

   NOTE: Show Slide 31.

   (1) The interface between the MCS and each of the loop modems is provided for the purposes of retrieving status from the modems and sending commands to the modems.
   (2) The loop modem interface consists of four TTL lines for each of the 48 modems.
   (3) Modem Loopback Command.

      (a) Sent from MCS to modem.
      (b) Causes modem to enter loopback mode.

   (4) Loopback Mode.

      (a) Sent from modem to MCS.
      (b) Indicates that the modem is in the loopback mode.

   (5) Loss of Receive Carrier.

      (a) Sent from modem to MCS.

(b) Indicates that the modem is not detecting a receive carrier signal.

(6) Loss of Transmit Carrier.

(a) Sent from modem to MCS.
(b) Indicates that the modem is not detecting a transmit carrier signal.

c. MCSU to MCSU Interface.

NOTE: Show Slide 32.

(1) Card Present.

(a) The card present signals are used by each MCSU to determine whether its role will be master or slave.
(b) If both lines are inactive, then the MCSU is the master; otherwise, it is a slave.

(2) Bus Request - When a slave MCSU wants to transmit on the ILI interface, it asserts its Bus Request line.
(3) Enable.

(a) The master MCSU responds to a bus request by asserting its Enable line to the requesting MCSU, providing that the interface is not being used or is not already requested by another MCSU.
(b) When the slave receives this Enable, it performs its transmission to the ILI.

(4) Reset.

(a) The master MCSU resets the bus by pulsing the Reset line.
(b) The receipt of this reset pulse causes all MCSUs to reset their Bus Request and Enable signals (if any

are set) and to cease any transmission to the ILI.

(c) This reset is performed under two conditions.

1. When an MCSU becomes the master (such as, if the original master fails or at power-up).
2. When a slave MCSU does not return the End Operation signal within 10 ms of being granted the bus (7) Physical Interface.

17H 50M

10. Practical exercise.

a. Explanation to students.

(1) You must correctly answer 14 of 20 written questions within 1 hour.
(2) When you are completed with the practical exercise have your instructor grade it for you.
(3) If it is not clear what you are required to do, ask your instructor for clarification.

b. Application by students.

(1) Correctly answer 14 of 20 written questions by filling in the blanks within 1 hour.
(2) When you are completed with the practical exercise have your instructor grade it for you.
(3) If it is not clear what you are required to do, ask your instructor for clarification.

c. Evaluation. Evaluate students ability to correctly answer 14 of 20 written questions within 20 minutes.

17H 55M

SUMMARY:

You have now completed your training on the Communications interface group (CIG) and how information is transferred from the equipment side of the COMSEC to the message processor. This information will aid you in troubleshooting message processing problems.

18H

END

This document supports Task Number 113-603-3217.

U. S. ARMY SIGNAL CENTER AND FORT GORDON
Fort Gordon, Georgia 30905-5180

LESSON PLAN

TITLE: Communication Interface Group (CIG) Fault Isolation

LEARNING OBJECTIVE:

Action: The student must be able to correctly identify and correct malfunctions within the CIG.

Conditions: Given an AN/TYC-39A, multimeter, oscilloscope, card extractor, TM 11-5805-790-12 and 34 series manuals, student handout and practical exercise 150-74G10/E01-LP02-PE.

Standard: The student must correctly isolate two out of three malfunctions within 30 minutes per fault and correctly answer 7 out of 10 questions on the AN/TYC-39A CIG.

SAFETY CONSIDERATIONS: Make sure equipment is powered down before making any electrical connections. Remove all jewelry before starting any procedures.

RISK ASSESSMENT: A risk assessment has been conducted on this unit of instruction and the risk level is deemed to be: LOW RISK.

RESOURCE NEEDS/ REFERENCES: AN/TYC-39A, multimeter, oscilloscope, card extractor, TM 11-5805-790-12 and 34 series manuals, student handout, overhead projector, slides 1-13, and practical exercise 150-74G10/E01-LP02-PE.

METHOD OF INSTRUCTION: Conference and Practical Exercise

TIME: 14.0 Hours

APPROVAL DATE: 1 DEC 97
DEVELOPER: SFC CARTAGENA
DIV. CHIEF: Jack P. Rondon

NOTES TO INSTRUCTOR:

1. Ensure that the classroom is available and properly set up and that all equipment and training resources are available and in working order.

2. Ensure that enough technical manuals and Student Guides are available and account for all transparencies.

3. Before the end of class, evaluate students on their ability to perform the learning objective.

4. State all safety notes as they appear throughout the lesson plan.

3M

INTRODUCTION:

Elapsed Time — The CIG is the only link between the outside subscriber and the message processor. The CIG basically troubleshoots itself. During this lesson you will be given the opportunity to troubleshoot the CIG.

BODY:

NOTE: Show Slide 1.

1. ILI Maintenance and Fault Isolation.

   a. Corrective Maintenance.

      (1) On-line Fault Detection.

         (a) Printouts are usually the first indication of a trouble/failure.
         (b) The results of on-line failure detection are indicated by mode status report printouts.
         (c) ILIOP Error Detection

            1. ILIOP constantly monitors itself for illogical conditions, including

exceptions detected by the 80386 microprocessor.

2. Upon detecting such a fatal error, the ILIOP performs the following.

NOTES: Refer students TM 11-5805-790-12-4 para 5-46 page 5-377. Mode Status Report Printouts, and discuss.

a. Reports to the MP via an error code in a mode status entity.
b. Illuminates the red LED on the ILIP circuit card.
c. Suspends all further processing.

3. The ILIOP also constantly monitors for recoverable, non-fatal error conditions.
4. Upon detecting a non-fatal error condition, ILIOP performs the following.

a. Reports to the MP via an error code in a mode status entity.
b. Performs recovery processing and continues with normal processing.

(d) System Alarm - "ILI" means at least one ILI is configured to the off-line DLC. This alarm is displayed on the VDT until all 13 ILIs are configured to the on-line processor. To determine which ILIs are connected to the MP, enter a STAT CFG command.

(2) off-line Testing - ILIP BIST.

NOTE: Show Slide 1.

(a) Diagnostics/BIST for the ILIP reside in ROM as a part of the ILIOP. BIST includes testing of the following.

1. CPU Test - The CPU test includes those tests necessary to verify operation of the 80386 microprocessor.
2. Random Access Memory (RAM) Test - The RAM test includes the following.

    a. Memory Range Test - Includes writing standard patterns to memory on a march through RAM and then verifying those patterns.
    b. Memory Addressing Test - Includes writing predetermined data to known addresses, verifying the content of those addresses, and also testing the different 386 microprocessor addressing modes.

3. Devices Test.

    a. Initialize DMA and SCC devices.
    b. Test the programmable interrupt controller.
    c. Initialize the programmable interval timer and verify the operation of the program timers.
    d. Place the SCC in loopback and test output transmission through it.

(b) BIST is initiated at power-up or reset.
(c) Test results are reported to the MP in the form of a Mode Status Report.
(d) The MP analyzes the BIST status word.
(e) If a failure occurs, a diagnose code is sent to the VDT and LTU.
(f) Summary pass/fail light on circuit card.

(3) on-line Testing.

NOTE: Show Slide 2.

(a) DATU Diagnostics.

10M

1. DATU Processing Unit (DPU) Test.

a. ILIOP initiates a DPU test, run by DATU Operational Program's Load and Test Code (DOP L&T), for any of its DATUs before it requests a download of DOP for that DATU.
b. ILIOP orders DOP L&T to start the test via a DPU test command, which can only be sent during the DOP Load and Test idle state.
c. Upon sending this command, ILIOP starts a 20-second timer.
d. If DOP receives this command in any state that is invalid, the command is not accepted, DOP remains in its present state, and a DOP RECOVERABLE ERROR DETECTED status is returned.

e. The DPU test command causes DOP L&T to perform diagnostics of the following DPU functions:

[1] Real-Time Clock (RTC).
[2] Read-Only Memory (ROM).
[3] Random Access Memory (RAM).

f. As each function is tested successfully,DOP L&T returns a RTC TEST PASS, ROM TEST PASS, and RAM TEST PASS, respectively.

g. If any test is unsuccessful, DOP L&T returns a TEST FAIL status report.

h. Upon successful completion of the DPU tests, DOP L&T returns to the DOP Load and Test Idle state.

i. If the 20-second timer expires or any test is unsuccessful, ILIOP must send the RESET command. It shall also report the test failure to the MP in the catalog segment.

j. If all the tests pass, the DPU test is considered to be successful and ILIOP proceeds with DOP load.

2. DATU Error Statues - DOP reports any internal illogical condition to ILIOP as an error

status, of which there are several. ILIOP reports these DOP detected errors in a mode status entity.

(b) CEF Control Channel Tests.

NOTE: Show Slide 3.

1. When requested to by the MP in an ACK List segment, ILIOP performs a series of tests on the Common Equipment Facility (CEF) Control Channel (CCC) through the active ICU and reports the results in a COMSEC diagnostics results entity.

2. The purpose of these tests is to verify the operation of the CCIU and the ICU, and to test for parity errors within the CEF.
3. There are nine subtests to be conducted.

   a. ICU test.
   b. Six CU tests.
   c. Rekeying Control Unit. (RCU) test.
   d. Idle test.

4. The tests are performed by sending sequences of ICU commands, and by validating CCIU status and ICU reports returned in response.
5. All nine subtests are run, regardless of the result of each subtest. The nine subtests may be run in any order.

NOTE: Refer students to Information Sheet D1-14, CCC Test Initiation/Results, and discuss.

(c) COMSEC Periodic Tests.

NOTE: Show Slide 4.

1. Every three minutes, ILIOP requests the status of the LKGs assigned to its in-service lines or, in the case of a line to an ICU, requests the status of the Rekeying Control Unit (RCU).
2. If a resulting status is not normal or if it is an RCU status, it is reported to the MP in an Equipment Report.
2. The initial status requests are made at a time based on the ILIP's physical location.

4. The algorithm for determining this time is designed to prevent all ILIPs in the system from requesting status at approximately the same time, yet ensure that all make their initial requests within three minutes of ILIOP initialization.

(d) Loopback Tests - There are six different loopback tests which may be requested by the MP.

NOTE: Show Slide 5.

1. Loopback tests are performed when requested by the MP in a channel parameters entity.
2. Information on whether a test is in progress and the test results are both returned to the MP in the catalog segment.
3. MCS Loopback Test.

NOTE: Show Slide 6.

a. ILIOP causes the MCS to perform a self-test by sending it an MCS test command.
b. ILIOP then waits for the test results, which are returned in three separate MCS Reports automatically generated by the MCS in response.
c. The test is considered to have passed if all three reports are received and indicate that the MCS self-test passed.

4. DLTU Loopback Test - ILIOP first classmarks the DLTU into loopback. The rest of the test procedure depends on the particular mode to which the DLTU has been classmarked.

NOTE: Show Slide 7.

a. Modes II and IV.

[1] ILIOP sends a data pattern to the DLTU.
[2] ILIOP sets a timer and waits for the test data to be returned.
[3] ILIOP compares data returned to the data sent out.
[4] ILIOP delays 0.2 seconds to ensure that no spurious data comes in.
[5] The test is considered to have passed if the data returned does not

differ in any way from the data sent out and if no characters are returned that were not sent out.

b. Mode V.

[1] ILIOP sends a data pattern. A single Control Character (CC) shall be initiated during transmission of the data stream. The CC shall consist of alternating 1s and 0s.

[2] ILIOP sets a timer and waits for test data to be returned.

[3] ILIOP compares the data returned to test data sent out. The returned test data shall consist of the transmitted data with a PAUSE character followed by the paired CC inserted in the data stream.

[4] ILIOP sends out a second single CC that is the one's complement of the first CC.

[5] ILIOP compares the CC returned with the CC sent out. It should be returned

in the same manner as the first CC.

[6] The test is considered to have passed if the returned data does not differ in any way from that expected.

c. For Mode I (after receiving a Sync achieved indication from the DLTU due to the loopback classmark).

[1] Block-by-Block Mode.

[a] ILIOP sends short line blocks of test data with the first framing character a Start of Header (SOH) and the third framing character an End of Transmission Block (ETB).

[b] ILIOP sets a timer and waits for the Line Block (LB) to be returned, followed by the proper block parity character.

[c] ILIOP compares the LB returned with the LB sent out and

the block parity returned with the computed block parity.

[d] ILIOP sends out a Start of Text-End of Text (STX-ETX) block with block parity computed to be the 1■s complement of the first block parity.

[e] ILIOP repeats steps (b) and (c).

[f] ILIOP sends out two single CCs. The second shall be the 1’s complement of the first.

[g] ILIOP compares the CCs returned with the CCs sent out.

[h] ILIOP repeats steps (f) and (g) for two double CCs.

[i] ILIOP sends a resync command and waits for sync achieved.

[j] This portion of the test is considered a success if all returned data is as expected.

[k] ILIOP initiates a Status Report Loopback Test if the test has passed to this point.

[2] Continuous Mode.

[a] ILIOP performs steps (a) through (d) of the block-by-block procedure.

[b] ILIOP sets a timer and waits for the STX-ETX LB to be returned.

[c] ILIOP verifies that all data for this LB was received properly, up to but not including the ETX.

[d] ILIOP sends a set release command to the DLTU and waits for ETX, block parity, and one SYN character.

[e] ILIOP verifies this data and then sends out an STX-ETX block with block parity

computed to be the 1's complement of the first block parity.

[f] ILIOP repeats previous steps (b) and (c).

[g] ILIOP causes the ILI bus interface logic to perform a terminate transmission operation on the DLTU.

[h] ILIOP performs steps (a) through (c) of the block-by-block procedure.

[i] ILIOP performs steps (f) through (i) of the block-by-block procedure.

[j] This portion of the test is considered a success if all returned data is as expected.

[k] ILIOP initiates a Status Report Loopback Test if the test has passed to this point.

5. DATU Loopback Test - The DATU loopback test consists of a test of the DATU lineside hardware.

It is run from a portion of DOP that is loaded into DPU memory,

so a DOP load will be requested and performed, if necessary, before running this test.

NOTE: Show Slide 8.

a. ILIOP first passes DOP, a Start Operation Program command, and then the classmark contained in the channel parameters.
b. The ILIOP orders DOP to start the test via a lineside hardware test command. Upon sending this command, ILIOP starts a 30-second timer.
c. After receiving the lineside hardware test command, DOP returns the Operation Diagnostics Started status report and enters the lineside diagnostics state in order to perform a test of the DATU's lineside hardware.
d. If the test performs successfully, DOP returns the Lineside Hardware Test Pass status report and returns to the inactive state.
e. Any failure during the test results in either a 30-second time-out or in DOP returning the lineside hardware test fail status report.
f. ILIOP must send a reset command to the DATU if a failed status is returned or a time-out occurs.

g. For the duration of this test there is no traffic on the line, no data is transferred to the ILIP, and no commands (except a Reset or Trap command) are accepted by DOP.

6. Modem Loopback Test - Tests all equipment on the line out to and including the modem.

NOTE: Show Slide 9.

a. Remove ILIOP notifies local ILIOP (ILI1) via a Route Message to place modem in loopback.
b. Local ILIOP instructs MCS to place modem in loopback.
c. MCS places modem in loopback.
d. MCS notifies local ILIOP which, in turn, notifies remote ILIOP that modem is in loopback.
e. Once in loopback, the line is synchronized and classmarks contained in the channel parameters are transferred to the LTU.
f. The loopback test itself depends on the type of LTU and the classmark of the line and is performed as described above.
g. For a DATU, an additional test (the remote DATU loopback test) is performed as described below.
h. After the tests, the remote ILIOP requests the local ILIOP, which in turn instructs the MCS to

place modem in normal-through.

The MCS returns status to local ILIOP which, in turn, returns status to remote ILIOP.

i. The test is considered to have passed if the modem can successfully be place into loopback, the tests pass, and the modem can be removed from loopback.

j. The test is considered to have failed if the modem can successfully be placed into loopback, the test fails, and the modem can be removed from loopback.

k. If the modem cannot be placed into or removed from loopback, the MP is notified of this loopback test result in the Catalog segment.

7. Remote DLTU Loopback Test - In this test, ILIOP tests the operation of the equipment on a line through the physical point of loopback.

NOTE: Show Slide 10.

a. This test is not allowed for a line with a CCIU attached or for an MCS line.

b. ILIOP synchronizes the line.

c. ILIOP then transfers the classmarks contained in the channel parameters to the LTU.

d. ILIOP performs the actual loopback test according

to the classmark of the line, using the same test patterns described above.

8. Remote DATU Loopback Test - In this test, ILIOP tests the operation of the equipment on a line through the physical point of loopback.

   a. This test is not allowed for a line with a CCIU attached or for an MCS line.
   b. ILIOP performs a loopback test on a DATU line to ensure the line continuity. It does not fail due to normal transmission environment bit errors associated with this line type.
   c. The test utilizes the Hardware Error Correction capability of the DATU to protect against transmission environment bit errors.
   d. The test pattern is designed to verify line continuity, not DATU functional performance. The following steps are executed.

      [1] The line is synchronized.
      [2] An appropriate error correcting DATU classmark is issued.
      [3] ILIOP allows for long line delays.
      [4] ILIOP sends a data pattern to the DATU.

[5] ILIOP sets a timer and waits for the test data to be returned.

[6] ILIOP compares data returned to the data sent out.

[7] The test is considered to be a success if the data returned is the same as that sent out.

NOTE: Refer students to Information Sheet D1-15, On-line Loopback Test Initiation/Results, and discuss.

(4) Fault Isolation.

(a) Flowchart.

NOTE: Refer students to TM-11-5805-790-12-8, para 11-1, page 11-5 to para 11-6, page 11-61, M&FI Flowchart, and discuss.

(b) M&FI Table.

NOTE: Refer students to TM-11-5805-790-12-8, para 11-6, page 11-65, M&FI BIST Diagnose Codes, and discuss.

(5) LRU Removal and Replacement.

NOTE: Refer students to TM 11-5805-790-12-6 para 7-24, page 7-50 and discuss.

30M

(a) The ILI circuit cards are located in rows 2 and 3 of the DLC/ILI nest.

1. Row 2.

a. ILIPs 1 through 7.
b. LTUs 0 through 23.

c. DLTU for MCS (204).
d. CCIU A (206 and 207).
e. CCIU B (225 and 226).
f. 12V Regulator (219).

2. Row 3.

a. ILIPs 8 through 13.
b. LTUs 24 through 47.
c. 12V Regulator (319).
d. CAPC (340).
e. SCGRT (Resistor Terminator (341).

(b) Removal/Replacement Procedures.

NOTE: Refer students to TM-11-5805-790-12-7 para 10-16, page 10-41. Circuit Card Removal/Replacement, and discuss.

(6) Repair Verification.

(a) Configure repaired ILIP to the on-line processor via DCON ILI command.
(b) Check for any abnormal indications/printouts.
(c) If a DLTM6/7/8/9 card has been replaced, perform appropriate loopback test on appropriate channel.
(d) If an ILIP card has been replaced, perform appropriate loopback test on every LTU in that group.
(e) If replacement card does not correct fault, reinstall original card.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

2. DLC Maintenance and Fault Isolation.

a. Preventive Maintenance.

b. Corrective Maintenance.

(1) On-line Fault Detection.

(a) Printouts are usually the first indication of a trouble/failure.
(b) The results of on-line failure detection are indicated by mode status report printouts.

NOTE: Refer students to Information Sheet D2-12, on-line Fault Detection Printouts, page 1, Mode Status Report Printout, and discuss.

(c) Other printouts that indicate a problem may exist are:

1. RLBK

NOTE: Refer students to Information Sheet D2-12, pages 2 through 4, RLBK Printouts, and discuss.

2. ERR

NOTE: Refer students to Information Sheet D2-12, page 5, ERR Printout, and discuss.

3. FAIL

NOTE: Refer students to Information Sheet D2-12, pages 6 and 7, FAIL Printout, and discuss.

4. RELD

NOTE: Refer students to Information Sheet D2-12, page 8, RELD Printout, and discuss.

(d) LEDs - Located on LCF and DLCP front panel.

NOTE: Show Slide 11.

1. BIST - (yellow) indicates that BIST tests are running.
2. USER - (red) indicates that BIST test failure.

3. RUN - (green) indicates that microprocessor is running.

(2) Off-line Testing. Off-line M&FI performs an MDL loopback test on the standby MDL. If the MDL loopback test is successful, the MP issues a DEV command to reset the standby Multibus II. The Multibus II reset causes the standby DLCP and LCF to run Built-In Self Tests (BISTs) to determine the hardware operational integrity.

(a) MDL Loopback.

1. MP sends MDL a DEV A0 command to place the MDL in loopback mode.

2. MP issues an OFR test word (four bytes) to the MDL in ABCD order.
3. MP reads and compares the ITR test word which is transposed to BADC order.

(b) DLCP BIST.

1. Diagnostics/BIST for the DLCP resides in ROM as a part of the DLCOP. BIST includes testing of the following.

a. CPU Test - The CPU test includes those tests necessary to verify operation of the 80186 microprocessor.
b. Random Access Memory (RAM) Test - The RAM test includes the following.

[1] Memory Range Test - Includes writing standard patterns to

memory on a march through RAM and then verifying those patterns.

[2] Memory Addressing Test - Includes writing predetermined data to known addresses, verifying the content of those addresses, and also testing the different 186 microprocessor addressing modes.

c. ROM.
d. Programmable Interrupt Controller.
e. Programmable Interval Timer (PIT).

f. Message Passing Co-processor (MPC).
g. DMA device.
h. Interconnect registers access.
i. Solicited/unsolicited message loopback test.

2. The above devices are tested in the mode in which they are utilized by DLCOP.
3. BIST is initiated at power up or reset.
4. Test results are reported to the MP in the form of a Mode Status Report.
5. The MP analyzes the BIST status word.
6. If a failure occurs, a diagnose code is sent to the VDT and LTU.

(c) LCF BIST. Diagnostics/BIST for the LCF card reside in ROM as a part of the LCFOP. BIST includes the CPU test, a Random Access Memory (RAM) test, and a comprehensive test of all associated devices.

1. CPU Test - The CPU test includes those tests necessary to verify operation of the 80186 microprocessor.
2. Random Access Memory (RAM) Test- The RAM test includes the following.

   a. Memory Range Test - Includes writing standard patterns to memory on a march through RAM and then verifying those patterns

   b. Memory Addressing Test - Includes writing predetermined data to known addresses, verifying the content of those addresses, and also testing the different 186 microprocessor addressing modes

3. Devices Test - This portion of BIST shall perform a comprehensive test on the following.

   a. Direct Memory Access (DMA).

b. Serial Communications Controller (SCC) via the direct I/O Processor device.
c. PSB Controller (Message Passing Co-processor (MPC)).
d. Interconnect registers access.
e. Solicited/unsolicited message loopback test.

4. Test results are reported to the MP in the form of a Mode Status Report.
5. The MP analyzes the BIST status word.
6. If a failure occurs, a diagnose code is sent to the VDT and LTU.

(3) Fault Isolation.

(a) Flowchart.

NOTE: Refer students to TM-11-5805-790-12-8, para 11-1, page 11-4 and para 11-7, page 11-73 M&FI Flowchart, and discuss.

(b) DDLC M&FI.

NOTE: Refer students to TM-11-5805-790-12-8, para 11-7, page 11-74 DDLC M&FI Diagnose Codes, and discuss.

(4) LRU Removal and Replacement.

NOTE: Show Slide 12.

(a) Because the circuit cards within the DLC card nest each have a P1 and a P2 connector, the DLC card nest is divided into four rows.

1. Row 1.

a. DLCP (P1 connector) (101).

b. MDL (P1 connector) (103).
c. LCF 1 (P1 connector) (105).
d. LCF 2 (P1 connector) (107).

2. Row 2.

a. Redundant DLCP (P1 connector) (201).
b. Redundant MDL (P1 connector) (203).
c. Redundant LCF 1 (P1 connector) (205).
d. Redundant LCF 2 (P1 connector) (207).

3. Row 3.

a. DLCP (P2 connector) (301).
b. MDL (P2 connector) (303).
c. LCF 1 (P2 connector) (305).
d. LCF 2 (P2 connector) (307).

4. Row 4.

a. Redundant DLCP (P2 connector) (401).
b. Redundant MDL (P2 connector) (403).
c. Redundant LCF 1 (P2 connector) (405).
d. Redundant LCF 2 (P2 connector) (407).

NOTE: Refer students to TM-11-5805-790-12-7, para 10-17, page 10-43 Circuit Card Removal/Replacement, and discuss.

(b) Removal/replacement of LCF, DLCP, or MDL circuit cards.
(c) Removal/replacement of PSB multibus.

NOTE: Refer students to TM-11-5805-790-12-7, PSB multibus removal/Replacement, and discuss.

(5) Repair Verification.

(a) Configure repaired DLC to the on-line processor.
(b) Check for any abnormal indications/printouts.
(c) Make repaired DLC available by means of a YAVL command.
(d) Close on-line DLC by means of a CLOS command.
(e) If replacement card does not correct fault, reinstall original card.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

3. MCS Maintenance and Fault Isolation.

a. Preventive Maintenance.

b. Corrective Maintenance.

(1) On-line Fault Detection.

(a) Printouts are usually the first indication of a trouble/failure.
(b) The results of on-line failure detection are indicated by mode status report printouts codes 40 through 52.

NOTE: Refer students to Information Sheet D3-9, Mode Status Report Printouts, and discuss.

(2) MCS Self-Test.

(a) The MCSU performs a self-test of its internal logic upon receipt of the "MCS Test" or "MCS Reset" command or at power-up.
(b) An indicator on the MCSU circuit card will light momentarily and then go off if the self-test passes.
(c) If the self-test fails, the indicator remains lit.

(3) MCS Loopback Test/DIAG.

NOTE: Refer students to Information Sheet D3-10, MCS Loopback/Diag Test Initiation/Results, and discuss.

(a) LPBK CHN 52 MCS or DIAG.
(b) ILIOP causes the MCS to perform a self-test by sending it an MCS test command.
(c) ILIOP then waits for the test results, which are returned in three separate MCS Reports automatically generated by the MCS in response.
(d) The test is considered to have passed if all three reports are received and indicate the MCS self-test passed.

(4) Fault Isolation.

(a) Flowchart.

NOTE: Refer students to TM-11-5805-790-12-8, para 11-6, M & FI Flowchart, and discuss.

(b) M & FI Table.

NOTE: Refer students to TM-11-5805-790-12-6, para 7-19, M & FI BIST Diagnose Codes, and discuss.

(5) LRU Removal and Replacement.

NOTE: Show Slide 13.

(a) The MCSU circuit cards are located in slots 338, 438 and 538 of the Modem/TDIGM nest.

1. MCSU0 (slot 338).
2. MCSU1 (slot 438).
3. MCSU2 (slot 538).

(b) Removal/Replacement Procedures.

NOTE: Refer students to TM-11-5805-790-12-6 para 7-19, Circuit Card Removal/Replacement, and discuss.

(6) Repair Verification.

(a) Place logical line 52 in-service using CISR command.
(b) Check for any abnormal indications/printouts.
1H (c) If replacement card does not correct fault, reinstall original card.

NOTE: Recapitulate key points. Ask questions to ensure student understanding of material covered.

4. Practical exercise.

a. Explanation to students.

(1) You must correctly answer 7 of 10 written questions within 30 minutes and correctly identify 2 out of 3 faults within 30 minutes per fault.
(2) When you are completed with the practical exercise have your instructor grade it for you.
(3) If it is not clear what you are required to do, ask your instructor for clarification.

b. Application by students.

(1) Correctly answer 7 of 10 written questions by filling in the blanks within 30 minutes and correctly isolate 2 out of 3 faults within 30 minutes per fault.
(2) When you are completed with the practical exercise have your instructor grade it for you.

(3) If it is not clear what you are required to do, ask your instructor for clarification.

c. Evaluation. Evaluate students ability to correctly answer 7 of 10 written questions

within 30 minutes and isolate two out of three faults within 30 minutes per fault.

13H 55M

SUMMARY

This concludes the lesson on the CIG fault isolation. The CIG is the only means of information getting to the message processor. You will be given a chance to practice isolating faults.

14H

END

This document supports Task Number 113-603-3217.

ANSWER KEY

1. A25A1, slot 3
2. ILI 11
3. DLCP on A25A1-10
4. 760000
5. ILI9 or ILIP
6. 3, A23
7. DLTM9
8. A1
9. YAVL, CLOS, NAVL
10. 52